ABSTRACT

The invention relates to a process for assigning tasks in a multiprocessor digital data processing system having a preemptive operating system, and an architecture for implementing the process. The system comprises processors (200-203, 210-213) capable of processing the tasks in parallel, divided into groups (200-201, 202-203). An elementary queue (5*a*, 5*b*) is associated with each of the processor groups (200-201, 202-203) and stores tasks to be executed. All the tasks to be executed (*T*1 through *T*10) are stored in a table (4). Each of the tasks (*T*1 through *T*10) of the table (4) is associated with one of the queues (5*a*, 5*b*) and each of the tasks stored in the queues (5*a*, 5*b*) is associated with one of the processors (200 through 201). The associations are made by sets of cross pointers (*p*200 through *p*203, *pp*5*a*, *pp*5*b*, *pT*1, *pT*5, *pT*10, *p*5*a*1 through *p*5*a*4, and *p*5*b*1 through *p*5*b*10). In an additional embodiment, according to several variants, a (re-)balancing of the load of the system among elementary queues is performed.

FIG. 4